A 0.18μM CMOS THERMOPILE READOUT ASIC IMMUNE TO 50 MRAD (SI) TOTAL IONIZING DOSE AND SINGLE EVENT LATCHUP TO 174 MEV-CM²/MG. G. Quilligan[1], S. Aslam[2], B. Lakew[2], J. DuMonthier[1], R. Katz[1] and I. Kleyner[1], [1]Instrument Electronics Development Branch, NASA Goddard Space Flight Center, Greenbelt, MD 20771, [2]Solar System Exploration Division, NASA Goddard Space Flight Center, Greenbelt, MD 20771.

Introduction: Radiation hardened by design (RHBD) techniques allow commercial CMOS circuits to operate in high total ionizing dose and particle fluence environments. Our radiation hard multi-channel digitizer (MCD) ASIC (Figure 1) is a versatile analog system on a chip (SoC) fabricated in 180nm CMOS. It provides 18 chopper stabilized amplifier channels, a 16-bit sigma-delta analog-digital converter (SDADC) and a controller. The MCD was evaluated at Goddard Space Flight Center's and Texas A&M University's radiation effects facilities and found to be immune to single event latchup (SEL) and total ionizing dose (TID) at 174 MeV-cm^2/mg and 50 Mrad (Si) respectively.

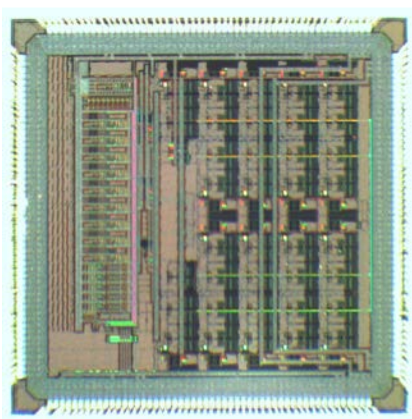

Figure 1. MCD ASIC (5mm x 5mm)

Thermal Imaging: Mapping the surface temperature anomalies and thermal inertia of a cold moon like Europa or Ganymede, from a space borne platform, requires the accurate measurement of the infrared spectral radiance [1]. A thermopile array converts the infrared radiation into microvolt-level signals which must be amplified, filtered and digitized with high signal-to-noise ratios (SNRs). The thermopile array is operated at cryogenic temperatures (≤ 170K) to minimize Johnson noise emanating from the relatively high output resistances of the thermopile pixels. The readout ASICs are placed in close proximity to the thermopile array to minimize parasitic effects and wiring. Together, the thermopile and readout ASICs form a detector focal plane assembly (FPA). Since thermopile arrays have been shown to be radiation hard to at least 10 Mrad [2], it falls upon the ASIC to also operate at high levels of ionizing radiation as well as at cryogenic temperatures so as to minimize the amount of shield mass of the FPA enclosure.

MCD Analog Signal Processor: The MCD [3] is a rad-hard analog signal processor/digitizer with multiple modes of operation. It can function as an analog multiplexer with buffering to an external application and an on-chip 16-bit SDADC; as a multi-channel variable gain instrumentation amplifier with/without chopper stabilization; as a chopper stabilized amplifier – integrator for extracting very small signals from sources with Johnson (thermal) noise. The latter application was the driver for the MCD's design as a radiation hard readout for a radiometer for the thermal mapping of icy moons in the Jovian orbital environment.

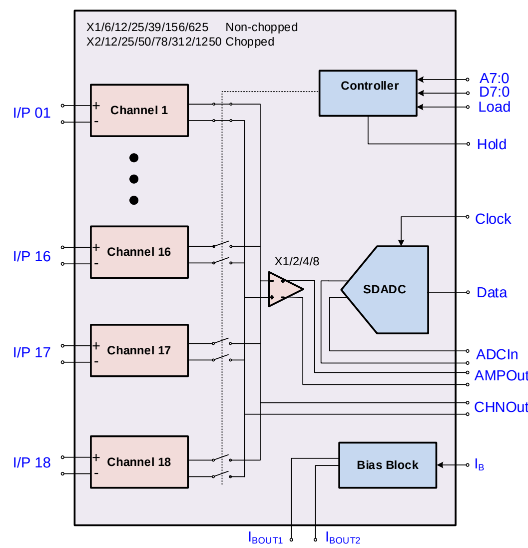

Figure 2. MCD block schematic

A block diagram of the ASIC is shown in Figure 2. Each channel utilizes a variable gain instrumentation amplifier (VGIA) to (1) present a high impedance to each thermopile pixel which has typically 10 kΩ of output resistance and (2) reject common mode noise. The MCD's amplifier channels create and maintain a differential signal path from the pixel inputs to the SDADC. Each channel amplifies its input signal with one of several gains either in chopped or non-chopped mode. If chopper mode is selected, the input signal is frequency translated to 125 kHz before amplification. Then the amplified signal is translated back to DC while at the same time any offset or 1/f noise in the amplifier is shifted up to harmonics of the chopper clock. The offsets and noise are then easily filtered at the output leaving just the amplified input signal. For filtering of thermal noise, the demodulated output signal can be passed through the channel's integrator which outputs to the SDADC through a post amplifier. The MCD chip also provides two die temperature sensor outputs in the form of MOS diodes biased by constant current sources. Each MOS diode voltage is an indicator of chip temperature. The supply current to the ASIC can also be varied to optimize power dissipation and speed. The first generation MCD ASIC utilized a parallel bus controller scheme. The second generation ASIC adds a serial interface facility allowing four wire control of the ASIC, although the parallel bus scheme is retained for direct addressing which is faster. The second silicon version will also increase the number of channels to 40 in the same 5mm x 5mm die size.

Radiation Effects: Standard CMOS circuit designs are sensitive to TID with failure modes resulting from increased leakage currents and, to a lesser degree in submicron CMOS nodes, threshold voltage variation. The leakage is predominantly due to parasitic currents between the NMOS devices' drain and source diffusions. It is caused by the inadvertent inversion of the P region under the shallow trench isolation (STI) on either side of the gate region in modern CMOS processes [4]. During exposure to ionizing dose, excess positive charge is deposited into the oxide layers above the N and P diffusions. Where overlapped by the polysilicon gate, this excess charge causes premature inversion and thus leakage in NMOS devices which in time can cause a circuit failure due to increased supply current and/or loss of isolation in CMOS switches.

The CMOS circuits are also at risk of latchup from energetic particle strikes (e.g. electrons or protons) causing turn-on of parasitic BJT devices in a thyristor like mode. SEL can destroy a device or at least impair its functionality and/or reliability. The only in-flight solution to a device in latchup is to cycle the power in an attempt to break the positive feedback loop which may restore functionality. Together, the TID induced leakage and SEL phenomena make operation near Europa extremely hazardous for unshielded standard CMOS based circuits.

Radiation hardness in an instrument's electronic circuits can be achieved with either shielding (e.g. aluminum) and/or robust electronic design/layout. The shielding while effective can add considerable mass to the instrument which increases the spacecraft's fuel requirements and thus the cost. Even with a reasonable amount of shielding, components must still be radiation tolerant with hardness to at least 300 krad. Radiation hardness of a circuit built in commercial CMOS can readily be achieved with a combination of layout [5] and circuit techniques. The MCD uses enclosed layout transistors (ELTs) primarily for the NMOS devices and selectively for the PMOS (in circuits which are sensitive to charge injection). The ELT removes the parasitic drain-source MOS effect causing leakage by enclosing either the source or drain N diffusion within the polysilicon gate. Double isolation rings around each transistor and every cell block give the ASIC its immunity to single event latchup. Layout techniques, however, do not impart complete immunity to radiation effects. The threshold voltage variation over many Mrad of ionization can alter the bias conditions in the circuits causing varying transconductance, Vdsat and increased amplifier offsets. Underpinning the other techniques described below, all bias circuits were designed to be robust to radiation induced threshold voltage changes. The amplifiers, as a result, are able to work with relatively wide supply voltage (1.2V to 2V) and supply current ranges. The MCD employs two circuit schemes to combat offset, both inherent and evolved due to TID. Chopper stabilization as described above is one such technique where the input signal is modulated and then demodulated either in the analog or digital domains which is a classic offset and 1/f noise reduction scheme. Chopper stabilization, however, does not prevent offsets affecting the frequency translated signal from saturating the analog signal chain. This is a possibility in circuits where the supply voltage is low and the gains are high. For example, a 1mV offset caused by TID could saturate an amplifier with a supply voltage of 1.8V and a gain of 2,000. To counter this effect, the MCD employs periodic auto-zeroing in each channel.

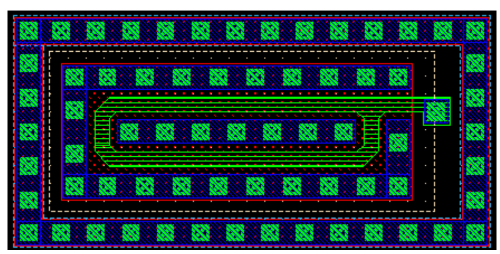
Figure 3. NMOS ELT device

Extensive radiation testing in 2013/2014 provided evidence of the chip's robustness to TID and SEL. It confirmed the efficacy of using a commercial CMOS process with RHBD techniques. Radiation testing was carried out at the Goddard Space Flight Center's radiation effects facility (REF) and at Texas A&M University's cyclotron facility. The following sections detail the methodology and the results.

Total Ionization Dose (TID) Tests: Three first-silicon parts (#5, #4 and #2), assembled in open cavity quad flat packages (OCQFP), were irradiated to 5 Mrad, 10 Mrad and 53 Mrad TID (respectively). All three parts continued to perform well both functionally and parametrically throughout and after irradiation. The goal was to identify any failure mechanisms due to ionizing dose radiation, simulating in part the predicted dosage accumulated by an unshielded ASIC in the thermal instrument in the Jovian system. The minimum TID requirement for the instrument is at least 2.7 Mrad (Si) behind 100 mils of aluminum [6].

Irradiation was performed with each device powered and clocked at 1MHz with supply current, propagation delay and the sigma-delta ADC (converting a mid-scale signal) all monitored continuously outside of the chamber. Each DUT (device under test) was irradiated individually on a socketed test board (also called the “bias board”) which had no potentially radiation-sensitive components (other than the DUT) installed on the printed circuit board (PCB). The bias board was installed in a Pb-Al ‘filter’ box to block low energy photons with the DUT’s die cavity facing the radiation source.

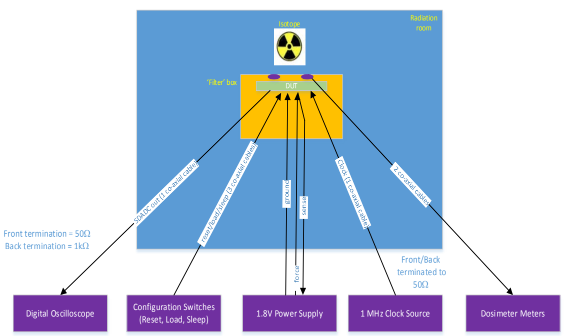

Figure 4. TID test setup

Ribbon and several coaxial cables led from the filter box through a notch in the top of the back wall (see Figure 4). The cables leading to the outside of the chamber were approximately 10 meters long. The cable carrying the clock signal into the chamber was 50 ohm coaxial and was front/back terminated into 50 ohms. The clock signal was monitored on an oscilloscope outside the chamber using the high impedance setting on an oscilloscope. The cable carrying the SDADC output signal was 50 ohm coaxial and was source terminated to 1k ohm and load terminated into 50 ohms. This arrangement reduced the effect of parasitic capacitances/inductances on the output signal and gave a relatively clean response with negligible reflections. Power and ground connections were supplied through a 40 lead ribbon cable. The power supply voltage to the DUT was 1.8V with force/sense connections at the DUT.

High dose rate was preferred for testing expediency. Two high precision dosimeters were utilized to verify the dose rate. The dosimeters consisted of read-out units and ionization chambers. The ionization chambers measured air KERMA (kinetic energy released per unit mass) to within a few percent [7]. A 5.5 krad/minute dose rate was selected in order to allow for uniform rate from one ionization chamber to the DUT to the second ionization chamber [7]. Several runs (irradiations) were performed.

Table 1. Irradiation data for the MCD TID Tests.

DUT #	Dose Rate (krad/min)	Duration (hours)	TID (krad)
5	5.49	15.27	**5031.6**
4	5.50	23.10	**10021.6**
2	5.50	161.83	**53356.4**

Part #4 was tested first and removed for parametric test at 2.4 Mrad and re-inserted to run to 10 Mrad. Since there were no significant changes in the in-situ tests of the other two parts, they were allowed to accumulate 5 Mrad and 53 Mrad uninterrupted. The end-point parametric tests measured each part’s transfer function, linearity and SNR with microvolt level signals applied. Post irradiation testing of the chip’s controller also indicated no degradation in that function. The fact that the linearity and noise gave reasonable results also indicated that the non-overlapping clock generators in both the controller and the SDADC were still working within specifications.

The parametric tests consisted of supply current (active and standby), chopper stabilized amplification at a very high channel gain of 25,000, integration time of 0.1s and digitization by the SDADC. The supply current for DUT #2 is plotted versus dose in Figure 5. The transfer functions for DUT #1 (control part) and DUT #2 are shown in Figure 6.

Table 2. Post TID radiation test data for the MCD.

DUT #	O/P Offset (mV)	Gain V/V	Non-Linearity %	SNR
1 (control)	+ 9.3	25,118	1.20	59
2	-57.4	25,725	0.85	49
4	-62.2	26,079	1.14	45
5	-59.6	26,984	1.17	49

As expected, all three irradiated parts exhibited increased offsets compared to the control. The three irradiated parts had offsets close to -2.2uV input referred, compared to the control of +0.37uV. The channel gains of the irradiated parts were also slightly increased compared to that of the control. The SNRs for all three irradiated parts were 17 to 24% lower than the control. Linearity was similar for all four parts.

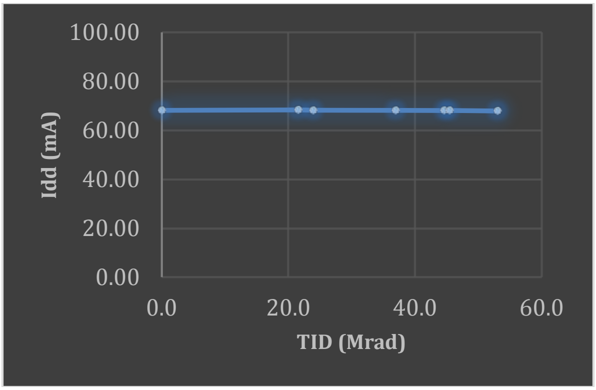

Figure 5. Supply current vs. total ionizing dose

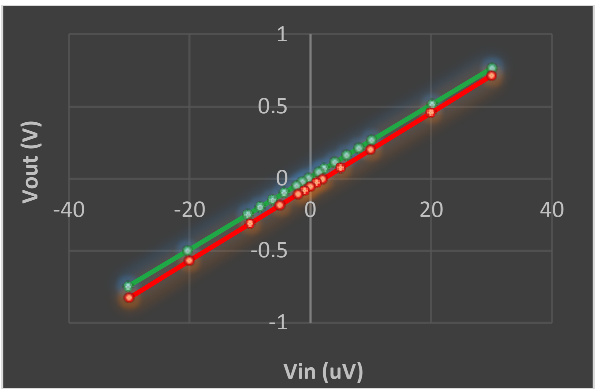

Figure 6. Gain curves for control (green) & 53 Mrad parts

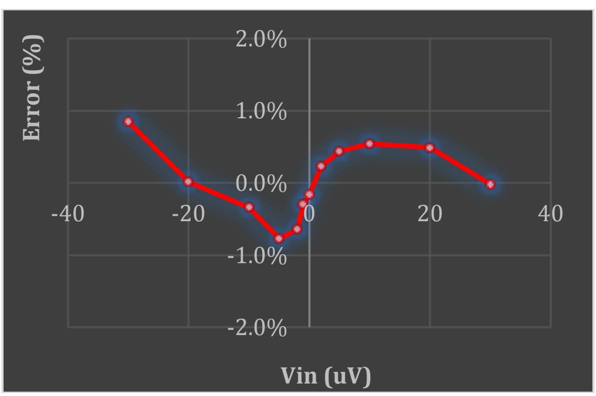

Figure 7. Gain non-linearity post 53 Mrad TID

Non-linearity for part #2 is illustrated in Figure 7 over the input range of ± 30uV (e.g. a 1% error is equivalent to a 0.6uV input referred inaccuracy). The SNR test was then repeated for a lower gain (1,000) on one of the irradiated parts and this is plotted versus the input voltage in Figure 8. SNR is higher at the lower (and more practical) channel gains. Integration times were 0.1s.

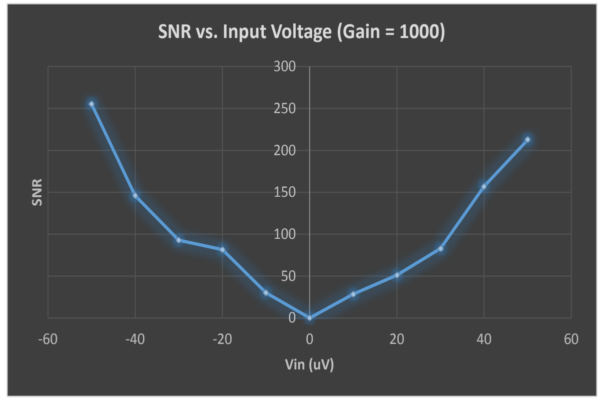

Figure 8. Post irradiation SNR vs. Vin

Heavy Ion Tests [8]: Three first silicon parts (#1, #2 and #3) were then tested for single event latchup and upsets at TAMU's cyclotron facility. One of the parts, DUT #2, was previously irradiated to 53 Mrad TID. All three parts continued to work well throughout the irradiation intervals with no evidence of latchup to an effective linear energy transfer (LET_{eff}) of 174 MeV-cm^2/mg. Each DUT was irradiated with its lid removed while operating continuously in a test board. The board was mounted on a Panavise on a platform which could be precisely positioned with respect to three axes close to the ion emitter (Figure 9).

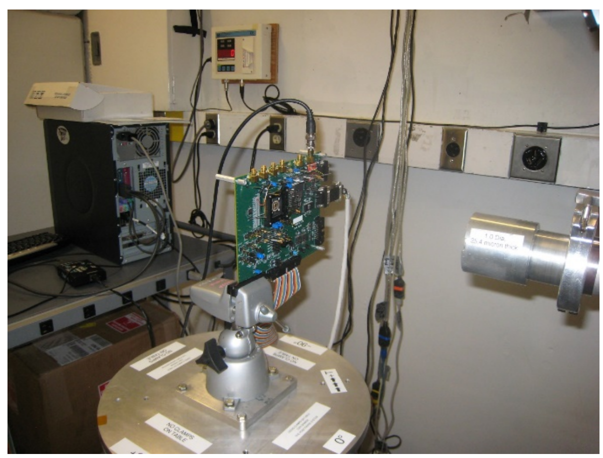
Figure 9. Test fixture set-up prior to heavy ion irradiation at TAMU cyclotron facility.

Each DUT’s supply current and SDADC output codes were continuously monitored during irradiation while amplifying and digitizing a mid-scale input signal. The standard auto-zero, chopping, integration, and digitization test sequence was applied. During each test sequence, the integrators were run continuously for 0.1s while being digitized by the SDADC and the sequence was repeated for at least the duration of the beam live time (time for which the beam was on). The supply voltage was set to 2.0V (maximum) while the chip was set to draw the maximum supply current through control of an external bias current into the chip. The power supply current was clamped at 20% above the expected maximum. All measurements were performed at room ambient temperature. Irradiation was performed with four ion species: Xenon, Gold, Krypton and Argon at varying beam angles to achieve the required effective LET values. The beam angle was varied to achieve a wide range of effective LET_{eff} from 8.7 to 174 MeV-cm^2/mg. For all three parts, no SEL occurred during the tests up to an LET_{eff} of 174 MeV- cm^2/mg with a fluence of 10^6 ions/cm^2 at T_A = 25°C.

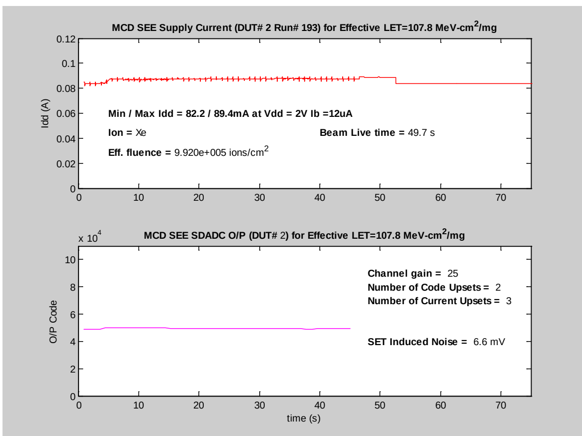

Figure 10. Supply current and output codes vs. time for an effective LET = 107.8 MeV-cm^2/mg

Figure 10 shows a plot of supply current and output codes versus time for DUT #2 during an irradiation run of 107.8 MeV-cm^2/mg. The channel gain in the figure refers to the pre-amplifier gain of 25, which is followed by gain stages which raise the total to 25,000. The beam live time was 49.7 seconds. In the supply current plot, the small 'glitches' are the result of the chopping action in the amplifier channels. Supply current varied slightly at beam turn on and turn off. In the MCD, single events can cause both SEUs and SETs (single event transients). SEUs are logic/register bit related errors, while SETs manifest as voltage and current spikes in the analog circuits which are amplified and appear as transients in the output codes and the supply current. For this analysis, a code upset was considered to have occurred if the difference between any two contiguous ADC measurements exceeded the standard deviation of all of the run's output values within the live beam time. SETs were monitored in two ways: as upsets in the nominal output codes and in the supply currents. An SET can appear as a supply current spike because the instrumentation amplifiers' output currents are a function of the output voltages and their feedback network resistances. A current upset or transient was deemed to have occurred if the difference between any two contiguous current measurements exceeded 500uA. Figure 11 shows an SEU cross section plot for DUT #2. The cross section is computed as "per channel". The cause of the roll-off in the cross section plot above 123 MeV-cm^2/mg is not understood at this time.

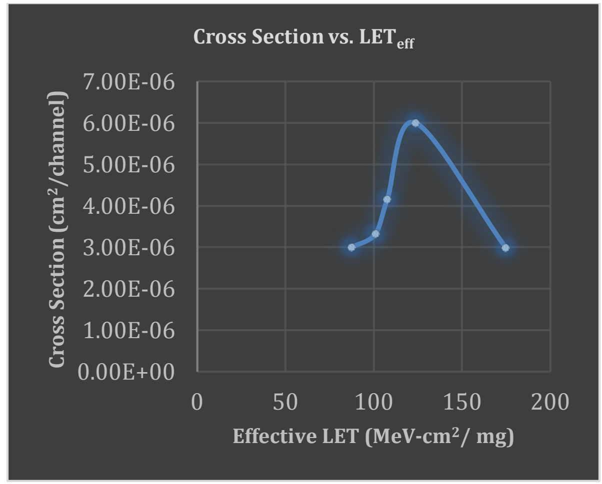

Figure 11. SEU Cross section vs. Effective LET for DUT #2

Nearly all SEUs or SETs would be recognizable in the output data stream given the DC nature of the thermopile signals. In an actual system, the chip's registers would be continually refreshed so SEUs would not result in persistent states. SETs would also be flushed out between chopper clock cycles and the averaging nature of the SDADC would also tend to filter them out.

Conclusions: Radiation testing on a custom thermopile readout ASIC fabricated in a commercial 180nm CMOS process indicated that the chip was immune to TID and SEL to greater than 50 Mrad and 174 MeV-cm^2/mg respectively. It showed that commercial CMOS process nodes can be hardened with a combination of layout and circuit design reducing the amount of shielding needed by a readout in the Jovian orbital environment. A second silicon version currently in design will double the number of channels and add a serial control interface.

References: [1] Hanel R. A. et al. (2003) *Exploration of the Solar System by Infrared Remote Sensing*. [2] Gaalema S. et al, (2010) *Proc. of SPIE*, vol. 7780. [3] Quilligan G. et al. (2012) *IWIPM, LPI Contribution No. 1683*, p.1095. [4] Rezzak N. et al. (2011) *Microelectronics Reliability*, vol. 51 889-894 [5] Chen L. and Gingrich M. (2005) *IEEE Trans. Nucl. Sci*, vol. 52 861-867. [6] *Europa Clipper Proposal Information Package* (2014) JPL D-92256, p. 21. [7] Carts M. (2014), *Internal GSFC Code 561 memorandum*. [8] Schwank J.R. et al. (2008) *Sandia National Laboratories Document SAND-2008-6851P*