A Radiation Hardened By Design CMOS ASIC For Thermopile Readouts

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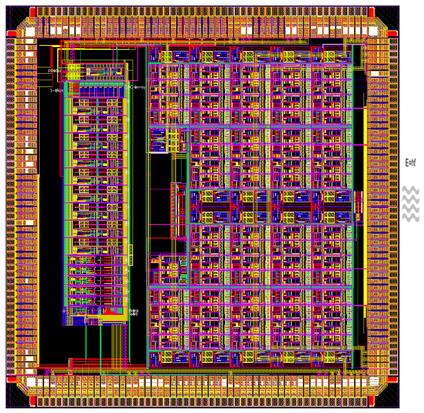
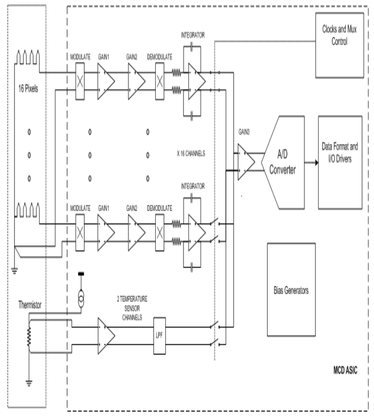
Introduction

NASA GSFC has developed a radiation hardened by design (RHBD) multi-channel digitizer (MCD) ASIC. Designed in TowerJazz Semiconductor's 180nm CA18HD commercial CMOS process, the 5mm x 5mm chip incorporates 16 chopper stabilized readout channels with 2 temperature sensor channels, a sigma-delta (SD) ADC and a controller. The channels have variable gains and integration times allowing the user to optimize the channel SNR for a wide range of input signal amplitudes. The design uses enclosed layout transistors to harden against total ionizing dose (TID) induced leakage and diffusion guardrings to prevent single event latchup (SEL). A radiation tolerant Nyquist16-bit ADC is also included on the ASIC.



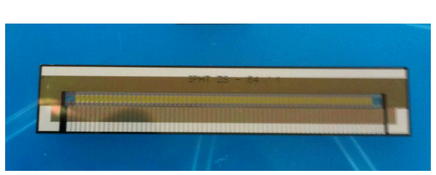
MCD die plot (5mm x 5mm)



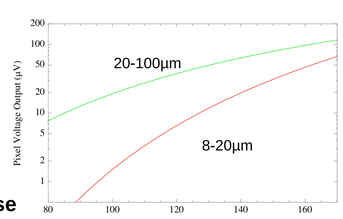
MCD application schematic

IR Measurement with Thermopile Arrays

Mapping the surface temperature of a cold moon like Europa or Ganymede requires the accurate measurement of the infrared spectral radiance. One sensitive measurement technique employs a filter radiometer that uses several thermopile linear arrays, with each array integrated with infra-red filters that have appropriate wavelength pass bands. The thermopile's microvolt level output signals are not large enough to be detected at a high enough SNR by even very high resolution ADCs (e.g. LSB=30uV). The tiny thermopile pixel voltage outputs must be amplified, filtered and digitized with minimum noise. Each pixel is processed by a dedicated amplifier channel while one ADC can be used to sequentially digitize the multiplexed channel outputs. The high channel count (~1024) dictates the use of ASICs to minimize the mass-volume-power (MVP) product. The ASIC can operate in TID environments of at least 3Mrad and at temperatures below 170K**.**

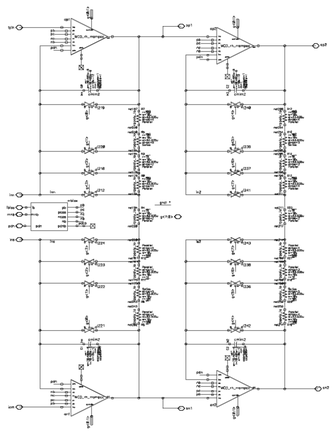


64 pixel thermopile array and output response



MCD Channel Topology

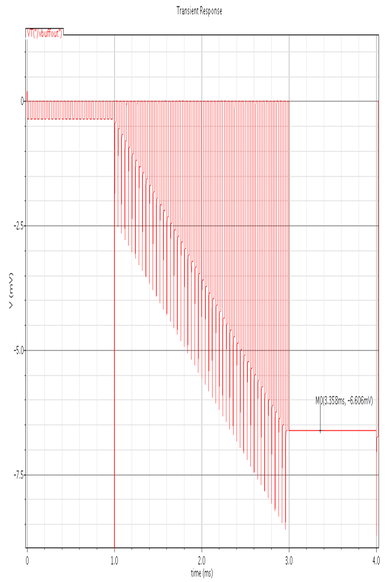
To scale a sub uV level signal to a value that can be processed by an ADC requires a gain of several thousand. This high a gain can result in saturation of the gain stages due to the presence of offsets. The MCD solves this problem by first modulating (or chopping) the pixel voltages, then amplifying followed by demodulating the result. The chopping process also reduces the 1/f noise inherent in the amplifier stages. The MCD employs a chopper stabilized instrumentation amplifier scheme that has variable gain and integration times with the option to turn off chopping and/or bypass the integrator. The channel outputs are selected by a multiplexer for output to the user as a buffered analog signal and for digitization by the on-chip SD or Nyquist ADCs. To maintain flexibility, the channels are bus addressable allowing channel specific amplification schemes. Each temperature sensor channel has an associated output current source allowing an array thermistor/diode to be biased. All timing signals are synchronized to an external clock which also serves as the modulator clock for the SD ADC.



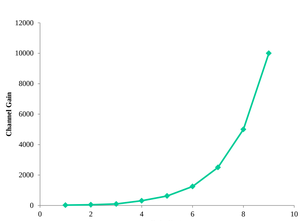
Variable Gain Instrumentation Amplifier

Parameter	Value
Supply voltage	1.80 V
Supply current	70 mA
Number of TP channels	16
Number of TS channels	2
Signal to noise ratio	> 256
TP input signal amplitude	0.1 – 120 µV
Gain (variable)	1 – 10k
Chopper frequency	40 - 125 kHz
Noise	<50 nV/√Hz
Ambient temperature	150 – 300 K
SDADC resolution	16 - 20 Bits
SD modulator clock rate	1 MHz
SD Nominal OSR	256
Pipeline ADC resolution	16
Pipeline ADC clock rate	1 – 20 MHz

MCD Specifications



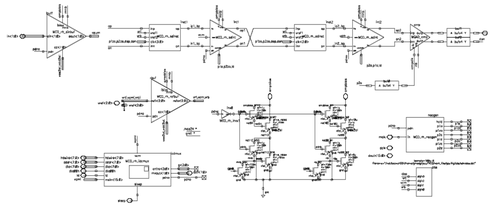
2ms integration of amplified 100nv input signal (x1250) followed by 1ms hold interval



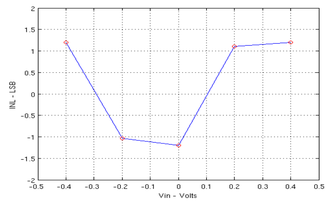
Channel gain versus user setting

On-Chip Sigma-Delta and Nyquist ADCs

The MCD ASIC contains two ADCs. One is a 2nd order SD ADC which outputs a single bit stream which is decimated off-chip to produce a resolution of at least 16 bits, depending on the oversampling ratio. This ADC is used to digitize the channel outputs and has a relatively low input bandwidth. The other ADC is a Nyquist 16-bit pipeline converter (PADC) with the ability to sample to 20MHz. The PADC can be used for digital averaging or general purpose house keeping tasks since its inputs (differential) are also directly accessible by the user. The SD ADC is a full RHBD implementation with immunity to at least 3Mrad. The Nyquist ADC is radiation *tolerant* with immunity to at least 300krad. The Nyquist ADC is on the left side of the chip (see die plot) and has separate supply, clock and input-output pins.



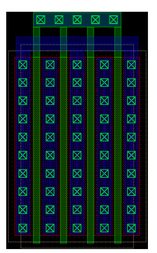
SDADC is RHBD (Fs=1MHz)



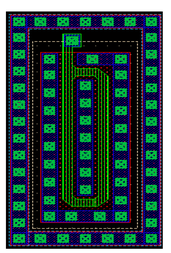
Channel + SDADC Linearity

Radiation Hardening by Design

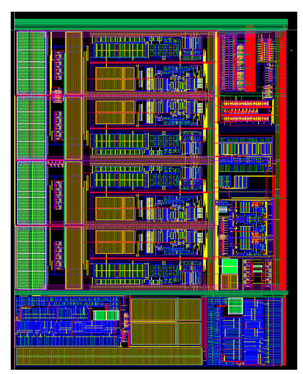
The MCD employs ELT NMOS in all circuits (except the PADC) to increase immunity to TID. In sampling circuits where charge injection affects the performance, ELT PMOS is also used, but the majority of the circuits use standard PMOS. The main leakage mechanism is at the STI oxide interface in standard NMOS so replacing with ELT NMOS virtually eliminates the TID induced leakage.



Standard NMOS



Guardringed ELT NMOS



RHBD channel with modulator, VGIA, demodulator and integrator

CONCLUSION

A prototype RHBD multi-channel digitizer ASIC in a commercial 180nm CMOS process has been developed. The ASIC is expected to perform as an amplifier-digitizer up to at least 3Mrad TID with immunity to SEL. The ASIC is currently being manufactured with parts available in December 2012.